This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1-31. (Canceled)

32. (Currently Amended) A semiconductor integrated circuit comprising: an HVMISFET (high withstand voltage MOSFET) having:

a source region and a drain region of a second conductivity type formed apart from each other on a surface of a semiconductor region of a first conductivity type,

a channel-forming region which is the surface of the semiconductor region between the source region and the drain region,

a gate formed on the channel-forming region via a gate insulating film,

the drain region being constituted of a low concentration drain region and a high-concentration drain region in contact with each other,

the low-concentration drain region being disposed between the channel-forming region and the high concentration drain region,

a field insulating film with a thickness at least one order of ten greater than that of the gate insulating film ~~formed by self-alignment~~ and located directly above the low-concentration drain region; and

a region diffused with elemental boron formed on the surface of the low concentration drain region and located directly between the field insulating film and the low concentration drain region[[.]]; and

an LVMISFET (low withstand voltage MOSFET) of the same conductivity type formed on the same semiconductor region and having the same threshold voltage and gate insulating film as the HVMISFET[[,]]

~~a surface concentration of the semiconductor region directly under the gate insulating film being partially increased to make the threshold voltage not less than 0.7 V, and~~

~~drain regions and source regions of the HVMISFET and the LVMISFET being constituted as phosphorus impurity regions.~~

33. (Previously Presented) A semiconductor integrated circuit according to claim 32, wherein the thickness of the gate insulating film is in the range of 100 to less than 200 Å.

34. (Currently Amended) A semiconductor integrated circuit according to claim 32, wherein the [[filed]] field insulating film and the low concentration drain region are formed from a common silicon nitride film.

35. (Previously Presented) A semiconductor integrated circuit according to claim 32, wherein the minimum gate length in the channel length direction of the LVMISFET is in the range of 1.5 – 2.5 μm.